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INFORMATION DISCLOSURE STATEMENT
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(See several sheets if necessary)

Applicant/Patent Owner: Osann Jr. et al.

Filing/Issue Date: April 5, 2001

Group Art Unit: 2825 2816

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
W	5,566,127	10-15-96	Hoshizaki	365	230.06	11-28-94
W	2. 5,572,148	11-05-96	Lytle et al.	326	41	03-22-95
W	3. 5,646,545	07-08-97	Trimberger et al.	326	38	08-18-95
W	4. 5,670,897	09-23-97	Kean	326	41	08-27-96
W	5. 5,708,597	01-13-98	Kelem	365	230.03	11-20-96
W	6. 5,715,197	02-03-98	Nance et al.	365	189.02	07-29-96
W	7. 5,732,407	03-24-98	Mason et al.	711	104	12-11-95
W	8. 5,744,980	04-28-98	McGowan et al.	326	40	02-16-96
W	9. 5,796,269	08-18-98	New	326	40	04-09-96
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W	11. 5,809,281	09-15-98	Steele et al.	395	497.01	01-28-97
W	12. 5,844,854	12-01-98	Lee	361	230.01	12-02-96
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W	16.	Matsumoto, C., LSI's SoC formula: FPGA plus ASICS, ELECTRONIC TIMES, 1999, n 1072, PG 1, 08-02-99.
W	17.	Souza, C., Programmable core opens door to SOC market, ELECTRONIC BUYERS NEWS, 1999, N 1171, PGS 08-02-99.
W	18.	LSI Logic to pry open market with FPGA core, ELECTRONIC NEWS, 07-29-99.
W	19.	Luca Carloni, Computer Science 294-7 Lecture #20 Compute Blocks, www.cs.berkeley.edu, spring 1997
W	20.	Afonso G. Ferreira and Siang W. Song, Achieving Optimality for Gate Matrix Layout and PLA Folding: A Graph Theoretic Approach, in <i>Latin '92, 1st Latin American Symposium on Theoretical Informatics, São Paulo, Brazil, April 6-10, 1992 Proceedings</i> , Simon, I. (Ed.), Springer-Verlag, Berlin, pp. 139-153.

Examiner

Date Considered

12/21/2001

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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